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EXAMINER	
MOORE, IAN N	

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2661	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/782,690	REDDY, NAVEEN S.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "a cache search controller" (claim 1, line 16; claim 12 line 22) and "antenna controller and modulator" (claim 1, line 4; claim 2, line 5), "a seed packet" (claim 1, line 17), "compatible packet" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.
2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show "table 40, cache skip flags 47", other labels whose labels recited in page 8-12 of the specification but not shown in the drawings, and their operation as detailed according to claims 1-26. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d).
3. The specification page 10, lines 20 discloses "...the cache cell ID search procedure is illustrated in Figure 3", however, the neither drawings nor the list of the drawing discloses Figure 3.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the

remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Spot beam hopping packet scheduler system in Satellite Communication.

Claim Objections

5. Claims 11, 14, 16,17,18,19,22 are objected to because of the following informalities. Appropriate correction is required.

- **Claims 11, 16,17,18,19,22** are **not** in a "**single sentence format**" since they includes periods "." Before the end of the claims (i.e. in claim 11, ..."...the spot beam hopping packet scheduler system as recited in claim 1, further comprising said cache skip flags to skip moving subsequent packet bursts from said downlink queue to said cache if the first packet burst for respective cell ID was not moved due to said respective cache FIFO

queue being full. Thus, the said skip flags preserve a first in first out (FIFO) packet burst order for a given destination Cell ID.)

- **Claim 14** recites, "...time slots expire **(**with....size**)**.." in line 4 and 8. For clarity, the **parenthesis** "( )" **should be removed** since the limitations within the parenthesis are still part of the claim.

Claim Rejections - 35 USC § 112- Second Paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites, "...said cache receiving and storing said downlink cell ID and burst memory pointers from said downlink queue... a downlink search controller...search said downlink queue **for packet bursts**, and fill any empty cache slots **with data** from said from said downlink queue...a cache search controller...a select a seed packet...assign **packet bursts** to spot beams..." in lines 12-19.

It is unclear whether "said downlink cell ID and burst memory pointers" or "packet bursts" is send from downlink search control to a cache.

It is unclear whether "data" refers to "said downlink cell ID and burst memory pointers" or "packet bursts".

It is unclear whether "packet bursts" produced by cache via the cache search controller is the same packet burst search by the downlink search controller.

Claims 12 and 23 are also rejected since they disclose the same limitations.

Claims 2-11,13-22,24-26 are also rejected since they depend on the rejected claims 1,12 and 23.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1,2,10, 12, 13, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Preito (U.S. 6,381,228), Liron (U.S. 5,930,254), and in view of Kudoh (U.S. 5,016,248).

Regarding claims 1 and 12, Prieto'228 discloses the satellite system (see FIG. 2, satellite network) having an apparatus for spot beam hopping packet scheduling (see FIG. 3, Media Access Controller 30), said apparatus receiving packets (see col. 7, lines 36-45; data and RQM cells) from a burst assembly and congestion controller (see FIG. 3, a combined system of ATM cell switch 28 and Flow-control module FCM 38; note that the combined system provide a capability of assembling, controlling and switching the cells), said

apparatus providing burst information to an antenna controller and modulators, said satellite system comprising:

a ground station (see FIG. 1 and 2, UET 10, User equipment terminal);

a satellite in orbit and in communication with said ground station (see FIG. 2, Satellite which is in communication with UET; see FIG. 3, satellite processing system 26), said satellite having an apparatus for spot beam hopping packet scheduling (see FIG. 3, Media Access Controller 30), comprising:

a downlink queue located in said satellite (see FIG. 5, Wholesaler queue 58 is within MAC 30) and coupled to said burst assembly and congestion controller (see FIG. 3, MAC 30 is connected to a combined system of ATM cell switch 28 and FCM 38), said downlink queue receiving and storing said packets (see FIG. 5, wholesaler queue 58 receive the packets from the switch and stores/backlogs them into a wholesaler queue 58; see col. 9, lines 40-46, 56-60);

a cache located in said satellite (see FIG. 6, Retail queue 60 has a capability to store the packets, this is a cache memory) and coupled to said downlink queue (see FIG. 4, retailer queue is connected to wholesaler queue), said cache receiving and storing said packets from said downlink queue (see FIG. 6, retail queue 60 receives packets from wholesale queue 58; see col. 10, lines 1-9);

a downlink search controller located in said satellite (see FIG. 5, PFQ-based scheduler 62 is located within MAC) and coupled to said downlink queue and said cache (see FIG. 5 and 6; PFQ-based 62 is connected to a wholesaler queue 58 and retail queue 60) said downlink queue search controller having control logic operative to search said downlink

queue for packet bursts, and fill any empty cache slots with data from said downlink queue (see FIG. 5, PFQ scheduler 62 searches for a particular wholesaler (i.e. A, B or C) from a wholesaler queue 58, selects the winner by utilizing packet fair queuing algorithm, and transmits the winner packet to retail queue 60 to fill any empty memory slots; see col. 9, lines 1-36, 56-64); and

a cache search controller located in said satellite (see FIG. 6, PFQ-based scheduler 64 is located within MAC) and coupled to said cache (see FIG. 6; PFQ-based 64 is connected to a retail queue 60), said cache search controller having control logic operative to select a seed packet selection from said cache with statistically weighted order (see FIG. 6, PFQ scheduler 64 searches for a particular retail user from a retailer queue 60, selects a winner from a retailer queue 60 by utilizing packet fair queuing algorithm which is the statistical weighted scheduling algorithm based upon statistical weighted attributes such as cost, rate, and bandwidth. PFQ algorithm is the pre-determined searching and scheduling algorithm based on order, range and weight of cost, rate, and bandwidth for different users and quality of service; see col. 44-55, see col. 10, lines 1-56), assign packet bursts to spot beams (see FIG. 6, DAMA replies to switch; see col. 8, line 10-12, see col. 13, lines 43-51; note that the when the winner request packet is selected, sport beam(s) channel/bandwidths are assigned by reserving and allocating the bandwidth, and the response is transmitted).

Prieto'228 does not explicitly disclose receiving downlink cell ID, and the selecting compatible packets from said cache.

However, the above-mentioned claimed limitations are taught by Liron'254. In particular, Liron'254 teaches a cached receiving downlink cell ID (see FIG. 1D, Routing

Cached memory 20 receives an extracted cell header with the cell address 21; see col. 7, lines 55-64), and

a cache search controller (see FIG. 1D, Input packet processor 28) coupled to said cache (see FIG. 1D, routing cache memory 20), select a seed packet from said cache (see FIG. 1E, an output port tag which corresponds the cell address is selected from Routing cache memory look up table, which contains the cell address and its associated port tag. The tag in each packet is used to form a series of cells which assigns to the an output beam port; see col. 9, lines 34-55)

select compatible packets from said cache (see FIG. 1D, each cells addresses which corresponds to the same tag is also selected since they are compatible with the same destination cell address; see col. 7, lines 45 to col. 8, lines 21), assign packets to spot beams (see col. 8, lines 8-15; note that each tag corresponds to output port for each beam or scanning beam antenna, SBA. When assigning a tag to the selected packet, it is assigning the packets to the beam; see col. 9, lines 34-55).

Note that Prieto'228 teaches selection packets with fair packet scheduling algorithm, which is the statically weighing scheduling algorithm. Liron'254 teaches selecting and assigning a tag for a packet with a particular cell address, then selecting subsequence packets and assigning compatible/same tag since they have compatible/same destination cell address. Thus, Prieto'228's queue controller can be modified with the teaching of Liron'254 to select compatible/same packets which have compatible/same destination address from the memory. In view of this, having the system of Prieto'228 and then given the teaching of Liron'254, it would have been obvious to one having ordinary skill in the art at the time the invention was

made to modify the system of Prieto'228, for the purpose of providing downlink cell address and selecting the same tagged cells with the same/compatible output beam, as taught by Liron'254, since Liron'254 states the advantages/benefits at col. 2, lines 20 to col. 3, lines 10 that it would optimize the utilization of network facilities and minimize transmission delay and variances of transmission delay. The motivation being that by selecting the packets according to the same destination cell address transmitting to the same output beam by utilizing the tag, it can increase the network throughput while reducing the cells switching processing time.

Neither Prieto'228 nor Liron'254 explicitly discloses storing burst memory pointers.

However, the above-mentioned claimed limitations are taught by Kudoh'248. In particular, Kudoh'248 teaches a queue stores burst memory pointers (see FIG. 6, address pointer queue 22 or 23 stores the plurality of pointers indication of areas of packets in RAM 100; see col. 4, line 39-55).

Note that the combined system of Prieto'228 and Liron'254 teaches storing cell address and packets in the downlink queue and cache. Kudoh'248 teaches the storing the pointers in the pointer queue, which corresponds to the packets in memory. Thus, the combined system of Prieto'228 and Liron'254 downlink queue and cache can be modified to store the memory pointer, per Kudoh'248 teachings. In view of this, having the combined system of Prieto'228 and Liron'254, then given the teaching of Kudoh'248, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Prieto'228 and Liron'254, for the purpose of providing a storing memory pointers in the pointer queue, as taught by Kudoh'248, since Kudoh'248

states the advantages/benefits at col. 3, lines 15-67 that it would provide an efficient use of the memory device. The motivation being that by utilizing the pointer queue, it can increase capability to locate where exactly the packets are in the memory in order to read or write, and by utilizing the pointer queue along with the memory, the memory space can be efficiently used since the pointers are stored in the separate queue.

Regarding claims 2 and 13, the combined system of Prieto'228, Liron'254, Kudoh'248 (and Hung'618 for claim 24 and 25) storing downlink cell ID and burst memory pointers as described above in claims 1 and 12 above. Liron'254 also discloses antenna controller (see FIG. Beam steering processor 86) and modulators (see FIG. 2, modulator 96); see col. 8, lines 54 to col. 9, lines 20. Liron'254 further discloses providing burst information (see col. 8, lines 8-15; a tag; note that each tag corresponds to output port for each beam or scanning beam antenna, SBA. When assigning a tag to the selected packet, it is assigning the packets to the beam; see col. 9, lines 34-55).

Kudoh'248 discloses a plurality of pointer output registers (see FIG. 6, transmission packet decider 80 comprises the shift registers) coupled to said cache (see FIG. RAM 100) and receiving burst memory pointers (see FIG. 6, receive pointer from pointer queue 23-1 to 23N), said plurality of pointer output registers providing information (see FIG. 6, transmission decider 80 provides address information regarding the transmitted packets); see col. 4, lines 50 to col. 5, lines 25).

In view of this, having the combined system of Prieto'228 and Liron'254, then given the teaching of Kudoh'248, it would have been obvious to one having ordinary skill in the art

at the time the invention was made to modify the combined system of Prieto'228 and Liron'254, as taught by Kudoh'248, for the same purpose and motivation as described above in claims 1 and 12.

Regarding claims 10 and 21, the combined Prieto'228, Liron'254, and Kudoh'248 discloses a cache as described above in claims 1 and 12. Prieto'228 further discloses said cache includes a plurality of memory locations (see FIG. 6, a memory/queue locations for Retailer user 1, 2, 3) each of said memory locations having a first in, first out queue (see FIG. 6, Retail user 1 has FIFO quantum queue).

In view of this, having the combined system of Prieto'228 and Liron'254, then given the teaching of Kudoh'248, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Prieto'228 and Liron'254, as taught by Kudoh'248, for the same purpose and motivation as described above in claims 1 and 12.

8. Claims 3 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prieto'228, Liron'254, and Kudoh'248, as applied to claim 1 and 12 (and Hung'618 for claim 26), above, and further in view of Yoshimura (U.S. 4,991,135)

Regarding claim 3 and 26, the combined Prieto'228, Liron'254 and Kudoh'248 disclose wherein said downlink queue as described above in claims 1, 12 and 23.

Neither Prieto'228, Liron'254, nor Kudoh'248 explicitly discloses wherein queue (see FIG. 2 and FIG. 4, Memory 9) includes a ping side (see FIG. 4, the first half of the memory location 10-1 to 10-4) and a pong side (see FIG. 4, the second half of the memory location

10-5 to 10-8), whereby said queue swaps, completing and restarting, said ping side and said pong side when Cache Depth/2 time slots expire (see FIG. 4, total memory is 10-1 to 10-8, where there is 8 time slots/intervals, where each half of memory time slot is 4 search in time slots/intervals; thus, note the system searches the first half of the memory location, and then search the second half of the memory location upon reaching 4 time slots/intervals; see col. 2, lines 50 to col. 5, lines 15; see col. 6, lines 51 to col. 7, lines 10, 54-67, and see col. 8, lines 1-10).

However, the above-mentioned claimed limitations are taught by Yoshimura'135. In view of this, having the combined system of Prieto'228, Liron'254 and Kudoh'248, then given the teaching of Yoshimura'135, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Prieto'228, Liron'254 and Kudoh'248, for the purpose of providing a memory searching mechanism where the first half and the second half of the memory is searching according to four time slots/intervals, as taught by Yoshimura'135, since Yoshimura'135 states the advantages/benefits at col. 2, lines 29-34 that it would provide fast searching feature as well as high rate of utilizing of its memory areas. The motivation being that by dividing the memory into two parts and searching them in order, it will reduce the searching time and overall storage capacity required.

9. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prieto'228, Liron'254, and Kudoh'248, as applied to claim 1 and 12, above, and further in view of well established teaching in art.

Regarding claim 4 and 15, the combined Prieto'228, Liron'254 and Kudoh'248 disclose wherein said cache storing cells IDs as described above in claims 1 and 12.

Neither Prieto'228, Liron'254, nor Kudoh'248 explicitly discloses a plurality of left hand pole Cell IDs and a plurality of right hand pole Cell IDs.

However, the above-mentioned claimed limitations are taught by well-established teaching in art. Well established teaching in art discloses a plurality of left hand pole Cell IDs and a plurality of right hand pole Cell IDs. Liron'254 disclose the cell addresses and FPS output port tags are stored in the table in the cache memory 20, see FIG. 1E. Note that it will well known in the art that each address can be grouped together according to their similarities, so that one can search the cell address easily. For example, it is well known in the art that file manager system in the PC, where grouping files into a folder so that one can easily search the file. Thus, each cell address is sorted and stored in the cache according to their cell addresses whether they are closed to right hand pole or left hand pole on the earth.

In view of this, having the combined system of Prieto'228, Liron'254 and Kudoh'248, then given the teaching of well established teaching in art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Prieto'228, Liron'254 and Kudoh'248, for the purpose of providing grouping of cell addresses according to their earth location (i.e. right or left of the pole), as taught by well established teaching in art. The motivation being that by grouping the cell address according to their similarities, it will increase the searching time since one can first easily identify the group name or address, in order to search an specific cell address.

10. Claims 5 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prieto'228, Liron'254, and Kudoh'248, as applied to claim 1, above, and further in view of Hung (U.S. 6,353,618).

Regarding claim 5, the combined Prieto'228, Liron'254 and Kudoh'248 disclose wherein said seed packet burst is selected across a pre-configured order, across a downlink cell range as described above in claims 1.

Neither Prieto'228, Liron'254, nor Kudoh'248 explicitly discloses wherein selected in a round-robin method (see Hung'618 FIG. 10, a scheduler 10 with round-robin algorithm), using a starting point for a search to find said seed packet burst by searching in a pre-configured seed search mode (see Hung'618 FIG. 4, step 32, the scheduler selects ideal slot for connection as a starting point for a search and selection according to pre-determine search and selection method), said seed mode consisting of Mode 1 seed and Mode 0 seed search (see Hung'618 FIG. 4, steps 34 and 36, the searching and selection method consists closest free slot preceding ideal slot method and the closet free slot after ideal slot method); see Hung'618 col. 5, lines 57 to col. 6, lines 30; see col. 7, lines 65 to see col. 8, lines 26).

However, the above-mentioned claimed limitations are taught by Hung'618. In view of this, having the combined system of Prieto'228, Liron'254 and Kudoh'248, then given the teaching of well established teaching in art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Prieto'228, Liron'254 and Kudoh'248, for the purpose of providing a round-robin schedule, which searches and selects the ideal slot by utilizing the search and select method, where method consist two selection steps: closest free slot preceding ideal slot method and the

closet free slot after ideal slot method, as taught by Hung'618 since Hung'618 states the advantages/benefits at col. 3, lines 4-25 that it would minimize the maximum burstiness or jitter of a packet stream. The motivation being that by utilizing a round-robin method for searching and selecting ideal slot, it will achieve the high switching rates while serving all the cells/packets fairly.

Regarding claim 23, Prieto'228 discloses a method of spot beam hopping packet scheduling (see FIG. 3, Media Access Controller 30 of the satellite network) comprising the steps of:

receiving downlink cells and storing said downlink cells in a downlink queue (see FIG. 5, wholesaler queue 58 receive the packets from the switch and stores/backlogs them into a wholesaler queue 58; see col. 9, lines 40-46, 56-60);

transferring said downlink cells to a cache (see FIG. 4, retailer queue 60 is connected to wholesaler queue; see FIG. 6, retail queue 60 receives packets from wholesale queue 58; see col. 10, lines 1-9);

preserving FIFO order for all bursts for a given Cell (see FIG. 6, a memory/queue locations for Retailer user 1, 2, 3, and each of said memory locations having a first in, first out queue (see FIG. 6, Retail user 1 has FIFO quantum queue));

searching said cache for seed packet burst in pre-configured search order, search range and statistical weighting (see FIG. 6, PFQ scheduler 64 searches for a particular retail user from a retailer queue 60, selects a winner from a retailer queue 60 by utilizing packet fair queuing algorithm which is the statistical weighted scheduling algorithm based upon

statistical weighted attributes such as cost, rate, and bandwidth. PFQ algorithm is the pre-determined searching and scheduling algorithm based on order, range and weight of cost, rate, and bandwidth for different users and quality of service; see col. 44-55, see col. 10, lines 1-56), assign packet bursts to spot beams (see FIG. 6, DAMA replies to switch; see col. 8, line 10-12, see col. 13, lines 43-51; note that the when the winner request packet is selected, sport beam(s) channel/bandwidths are assigned by reserving and allocating the bandwidth, and the response is transmitted);

searching said downlink queue for packet bursts; and filling any empty cache memory with data from said downlink queue (see FIG. 5, PFQ scheduler 62 searches for a particular wholesaler (i.e. A, B or C) from a wholesaler queue 58, selects the winner by utilizing packet fair queuing algorithm, and transmits the winner packet to retail queue 60 to fill any empty memory slots; see col. 9, lines 1-36, 56-64).

Prieto'228 does not explicitly disclose receiving downlink cell ID, and the selecting compatible packets from said cache.

However, the above-mentioned claimed limitations are taught by Liron'254. In particular, Liron'254 teaches a cached receiving downlink cell ID (see FIG. 1D, Routing Cached memory 20 receives an extracted cell header with the cell address 21; see col. 7, lines 55-64), and

a cache search controller (see FIG. 1D, Input packet processor 28) coupled to said cache (see FIG. 1D, routing cache memory 20), searching said cache for a seed packet in pre-configured search order and search weight (see FIG. 1E, an output port tag which corresponds the cell address is searched and selected from Routing cache memory look up

table, which contains the cell address and its associated port tag according to predefined search order and range. The tag in each packet is used to form a series of cells which assigns to the an output beam port; see col. 9, lines 34-55)

searching said cache for compatible packets bursts in preconfigured order and search rang (see FIG. 1D, each cells addresses which corresponds to the same tag is also selected since they are compatible with the same destination cell address. Thus, they are also searched and selected according to predefined search order and range; see col. 7, lines 45 to col. 8, lines 21).

Note that Prieto'228 teaches selection packets with fair packet scheduling algorithm, which is the statically weighing scheduling algorithm. Liron'254 teaches selecting and assigning a tag for a packet with a particular cell address, then selecting subsequence packets and assigning compatible/same tag since they have compatible/same destination cell address. Thus, Prieto'228's queue controller can be modified with the teaching of Liron'254 to select compatible/same packets which have compatible/same destination address from the memory. In view of this, having the system of Prieto'228 and then given the teaching of Liron'254, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Prieto'228, for the purpose of providing downlink cell address and selecting the same tagged cells with the same/compatible output beam, as taught by Liron'254, since Liron'254 states the advantages/benefits at col. 2, lines 20 to col. 3, lines 10 that it would optimize the utilization of network facilities and minimize transmission delay and variances of transmission delay. The motivation being that by selecting the packets according to the same destination cell address transmitting to the same output beam by

utilizing the tag, it can increase the network throughput while reducing the cells switching processing time.

Neither Prieto'228 nor Liron'254 explicitly discloses storing burst memory pointers.

However, the above-mentioned claimed limitations are taught by Kudoh'248. In particular, Kudoh'248 teaches a queue stores burst memory pointers (see FIG. 6, address pointer queue 22 or 23 stores the plurality of pointers indication of areas of packets in RAM 100; see col. 4, line 39-55).

Note that the combined system of Prieto'228 and Liron'254 teaches storing cell address and packets in the downlink queue and cache. Kudoh'248 teaches the storing the pointers in the pointer queue, which corresponds to the packets in memory. Thus, the combined system of Prieto'228 and Liron'254 downlink queue and cache can be modified to store the memory pointer, per Kudoh'248 teachings. In view of this, having the combined system of Prieto'228 and Liron'254, then given the teaching of Kudoh'248, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Prieto'228 and Liron'254, for the purpose of providing a storing memory pointers in the pointer queue, as taught by Kudoh'248, since Kudoh'248 states the advantages/benefits at col. 3, lines 15-67 that it would provide an efficient use of the memory device. The motivation being that by utilizing the pointer queue, it can increase capability to locate where exactly the packets are in the memory in order to read or write, and by utilizing the pointer queue along with the memory, the memory space can be efficiently used since the pointers are stored in the separate queue.

Neither Prieto'228, Liron'254, nor Kudoh'248 explicitly discloses selecting a starting point for seed packet burst (see Hung'618 FIG. 4, step 32, the scheduler selects ideal slot for connection as a starting point for a search and selection according to pre-determine search and selection method); see Hung'618 col. 5, lines 57 to col. 6, lines 30; see col. 7, lines 65 to see col. 8, lines 26).

However, the above-mentioned claimed limitations are taught by Hung'618. In view of this, having the combined system of Prieto'228, Liron'254 and Kudoh'248, then given the teaching of well established teaching in art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Prieto'228, Liron'254 and Kudoh'248, for the purpose of providing a starting point to select the ideal slot, as taught by Hung'618 since Hung'618 states the advantages/benefits at col. 3, lines 4-25 that it would minimize the maximum burstiness or jitter of a packet stream. The motivation being that by utilizing a round-robin method for searching and selecting ideal slot, it will achieve the high switching rates while serving all the cells/packets fairly.

Regarding claims 24 and 25, the combined system of Prieto'228, Liron'254, Kudoh'248 and Hung'618 storing downlink cell ID and burst memory pointers as described above in claims 23 above. Liron'254 also discloses antenna controller (see FIG. Beam steering processor 86) and modulators (see FIG. 2, modulator 96); see col. 8, lines 54 to col. 9, lines 20. Liron'254 further discloses providing burst information (see col. 8, lines 8-15; a tag; note that each tag corresponds to output port for each beam or scanning beam antenna,

SBA. When assigning a tag to the selected packet, it is assigning the packets to the beam; see col. 9, lines 34-55).

Kudoh'248 discloses a plurality of pointer output registers (see FIG. 6, transmission packet decider 80 comprises the shift registers) coupled to said cache (see FIG. RAM 100) and receiving burst memory pointers (see FIG. 6, receive pointer from pointer queue 23-1 to 23N), said plurality of pointer output registers providing information (see FIG. 6, transmission decider 80 provides address information regarding the transmitted packets); see col. 4, lines 50 to col. 5, lines 25).

In view of this, having the combined system of Prieto'228 and Liron'254, then given the teaching of Kudoh'248, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Prieto'228 and Liron'254, as taught by Kudoh'248, for the same purpose and motivation as described above in claims 23.

11. Claims 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prieto'228, Liron'254, and Kudoh'248, as applied to claim 1, above, and further in view of Takeda (U.S. 5,940,411).

Regarding claims 9 and 20, the combined Prieto'228, Liron'254 and Kudoh'248 disclose wherein said burst packet is extracted from said downlink queue as described above in claims 1.

Neither Prieto'228, Liron'254, nor Kudoh'248 explicitly discloses a shuffling method (see Takeda'411; see col. 2, lines 35-67; a shuffling method).

However, the above-mentioned claimed limitations are taught by Takeda'411. In view of this, having the combined system of Prieto'228, Liron'254 and Kudoh'248, then given the teaching of well established teaching in art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Prieto'228, Liron'254 and Kudoh'248, for the purpose of providing a shuffling method, as taught by Takeda'411 since Takeda'411 states the advantages/benefits at col. 2, lines 20-50 that it would provide the optimum shuffling method and has high concealment capability with respect to data error. The motivation being that by utilizing the shuffling method, it will reduce the error and increase the processing speed since the various cells/packets are rearranged and processed in the predetermine order with shuffling method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on 703-308-7828. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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8/30/04

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